Cerebras WSE-3

Wafer Scale Engine 3 | Wafer-Scale | 2024 | TSMC 5nm

OVERVIEW

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FP32 TFLOPS	VRAM On-die SRAM	Memory Bandwidth	TDP

PERFORMANCE METRICS

Precision	Peak TFLOPS	Bits	Type

MEMORY SPECIFICATIONS

Capacity	—
Type	On-die SRAM
Bandwidth	—
Interface Width	—

POWER & EFFICIENCY

TDP	—
Est. Max Power	—
FP32 Efficiency	—
FP16 Efficiency	—

HARDWARE DETAILS

Vendor: Cerebras

Architecture: Wafer Scale Engine 3

Process Node: TSMC 5nm

Form Factor: Wafer-Scale

Launch Year: 2024

COMPUTE ENGINE

Sparse linear algebra core:
900,000

CHIP DESIGN

Transistors: 4000.0 billion

Die Size: 46225 mm²