

Meta MTIA 200

MTIA

2024

5nm

OVERVIEW

— FP32 TFLOPS	128 GB Memory LPDDR5	205 GB/s Memory Bandwidth	90 W TDP
------------------	-------------------------	------------------------------	-------------

PERFORMANCE METRICS

Precision	Peak (dense)	2:4 Sparse	Bits	Type
FP64	—	N/A	—	Standard
FP32	—	N/A	32	Standard
TF32	—	not published	—	Standard
BF16	177.0	354.0	16	Standard
FP16	177.0	354.0	16	Standard
FP8	—	not published	—	Standard
FP6	—	not published	—	Standard
FP4	—	not published	—	Standard
INT8	354.0	708.0	8	Standard

MEMORY SPECIFICATIONS

Capacity	128 GB
Type	LPDDR5
Bandwidth	205 GB/s
Interface Width	—

POWER & EFFICIENCY

TDP	90 W
Max power (Flopper estimate)	~103 W est.
FP32 dense TFLOPS per W of TDP	—
FP16 dense TFLOPS per W of TDP	1.97 TFLOPS/W
Flopper estimate: 90 W TDP x 1.15. The vendor publishes no maximum board power for this part. Per W of TDP figures divide dense peak by accelerator TDP. Board power only; excludes host CPUs, networking, cooling and facility overhead.	

HARDWARE DETAILS

Vendor: Meta	Architecture: MTIA	Process Node: 5nm
Form Factor: —	Launch Year: 2024	

COMPUTE ENGINE

INTERCONNECT

PCIe: 5.0 x8

CHIP DESIGN

Die Size: 421 mm²

Chiplets: 1 (Monolithic)

ENTERPRISE FEATURES

Sparsity: Yes